REMARKS

An RCE and an IDS have been filed along with this amendment. Reconsideration and allowance are respectfully requested.

Claims 43, 45-53, 55-62 remain rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. This rejection is respectfully traversed.

Claim 43 recites: "A computer program product including a storage medium readable by a data processing apparatus encoded with instruction code which, when executed by the data processing apparatus, controls the data processing apparatus to execute a sequence of variable length instructions stored within a plurality of discrete memory address regions within a memory of said data processing apparatus." The claim is not to a program per se. The product includes instruction code embodied in a storage medium readable and executable by a data processing apparatus to achieve useful, concrete and tangible results. There is no requirement under 35 U.S.C. §101 that "specific elements of the program product be reflected into the claim body." Nevertheless, claim 43 has been amended to recite in the body of claim 43 specific code elements which, when executed by the data processing apparatus, control the data processing apparatus to perform useful, concrete, and tangible functions.

Applicants traverse the Examiner's conclusion that "no useful, concrete and tangible results can be determined." The rejected claims are concerned with how a data processing apparatus handles fragmented instructions (page 2, line 4-7 and page 3, lines 1-3). Although fragmented instructions can be desirable (e.g. for enhanced security), they also are associated problems such as memory aborts (see page 8, lines 21-24). The computer program product recited in claims 43, 45-53, 55-62 enables a data processing apparatus to handle such situations, and thus, to operate more efficiently. Certainly, given the central role that data processing

apparatus have in daily activities of most people in the industrialized world, enabling data processing apparatus to operate more efficiently is a useful, concrete, and tangible result of claims 43, 45-53, 55-62.

The Examiner suggests on page 4 of the final rejection that claims 43, 45-53, 55-62 are "computer programs claimed as computer listing per se." A review of the language used in claims 43, 45-53, 55-62 reveals that these claims are clearly not computer listings. Moreover, claim 43 clearly includes language that describes a functional relationship with a storage medium readable by a data processing apparatus. The claim explicitly recites code elements, which when executed by the data processing apparatus, controls the data processing apparatus to perform useful, concrete, and tangible functions. These specifically recited functional interrelationships between the code and other elements of a computer (storage medium and data processor) permit the computer code's functionality to be realized.

The Examiner misapplies the Interim guidelines when referring to page 53. That section of the guidelines is directed only to data structure representing descriptive material per se—clearly not the subject matter of claim 43—and computer programs representing computer listings per se. Applicants do not understand how the Examiner can be characterizing the text of claim 43 as a computer listing per se. There is not even a single computer instruction included in claim 43. Moreover, later on page 53 of the Interim Guidelines, Examiners are instructed that "a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory." The language used in claim 43 very closely tracks the language quoted above and certainly recites a computer-readable medium encoded with a computer program. Thus, the

very authority that the Examiner cites actually mandates that the computer-readable medium encoded with a computer program recited claim 43 is statutory.

The rejection of claims 43, 45-53, 55-62 under 35 U.S.C. §101 is improper and should be withdrawn.

Most of the claims remain rejected for anticipation under 35 U.S.C. §102 based on USP 5,598,544 to Ohshima. This rejection is respectfully traversed.

The technology of this application is directed to data processing systems that can execute a variable length instruction stored in distinct memory locations. The first part of a variable length instruction is stored in a first memory location, and the second part of the instruction is stored in a second different memory location. A "fix-up" memory address region is used to bring together the two parts of the single instruction. When a two-part, variable-length instruction occurs, the program execution flow is temporarily diverted to the fix-up memory to read the freshly reconstructed variable length instruction stored there. Thereafter, the program execution flow is returned to reading from the normal memory.

Ohshima is concerned with a very different problem: efficient processing of an instruction that includes both basic and expanded segments. A basic segment contains a code indicating the type of instruction (basic or expanded), and an expanded segment contains information relevant to the type of instruction specified by the basic segment. One instruction is formed from one or more basic and expanded segments. See column 3, lines 31-40. Even though the basic segments have a known length, the length of expanded segments can vary, and this length is not known until its corresponding basic segment has been decoded. Hence, in a situation where one of Ohshima's instructions consists of two basic segments and the first basic segment is followed by an expanded segment, the second basic segment cannot be input into a

decoder until after the first basic segment has been decoded, which allows the length of the expanded segment to be determined. Thus, two cycles are required to decode the single instruction. See column 2, line 59 to column 3, line 9.

Given that Ohshima does not even consider the problem of executing variable length instructions which span two discrete memory address regions, it is no surprise that Ohshima fails to disclose a number of features recited in the independent claims. A detailed discussion of those missing features was set forth in the prior response. Here, Applicants focus on selected deficiencies in response to the Examiner's remarks.

The Examiner maps the basis segments 1 and 2 shown in Figure 2 onto portions of a variable length instruction spanning two discrete memory address regions. The claimed concatenation is read onto Ohshima's wrapping of instructions within the instruction buffer 2 shown in Figure 4. As described above, Ohshima forms an expanded version of the instruction onto the instruction code bus ready for decoding and execution. The Examiner seems to be mapping this instruction code bus to the claimed fix-up memory address region. Applicants respectfully submit that a person skilled in the data processing art would not reasonably equate Ohshima's instruction code bus to the claimed fix-up memory address region—a bus and a memory are two different things with two different functions and operations.

The Examiner maps the claimed diverting and restoring to execution of an instruction on the instruction code bus and the execution of the next instruction. This mapping is also unreasonable. The instruction code bus is not part of the memory address space. Moreover, instruction decoding always takes place from Ohshima's instruction code bus, and as a result, there is no need to divert program execution flow to the instruction code bus or restore program execution flow from the instruction code bus.

The claim element mapping onto Ohshima attempted by the Examiner is not a reasonable mapping, and in any event, ultimately does stand up to a close analysis. Accordingly, the application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

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